UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/570,236	02/28/2006	Pieter Van Der Wolf	NL031032	2510

24737 7590 09/05/2007

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
P.O. BOX 3001
BRIARCLIFF MANOR, NY 10510

EXAMINER	
GIARDINO JR, MARK A	
ART UNIT	**PAPER NUMBER**
2109	

MAIL DATE	DELIVERY MODE
09/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/570,236	VAN DER WOLF ET AL.	
	Examiner	Art Unit	
	Mark A. Giardino	2100	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *1* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/28/2006.*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim 1 objected to because of the following informality: the word 'issuing' is misspelled. Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 rejected under U.S.C. 102(b) as being anticipated by Sindhu (US 5,440,698).

Regarding Claim 1, Sindhu teaches a data processing system, comprising a memory means (main memory 13 and controller 25) and a plurality of data processing means (processors 12 and cache 16) provided for accessing to said memory means (main memory 13 and controller 25), characterized by a communication interface means coupled between said memory means and said plurality of data processing means, said communication interface means including a network of nodes (controllers 21 and busses 15), each node comprising at least one slave port for receiving a memory access request from a data processing means or from a previous node (connections from the processor cache 16 to the bus 15) and at least one master port (connection from controller 21 to bus 26) for issuing a memory access request to a next node or to said memory means in accordance with the memory access request received at said slave port, wherein said at least one slave port (slave port of node containing bus 15) is connected to a master port of a previous node or to one of said data processing means

(processing means 16) to and said at least one master port (master port of node containing controller 21) is connected to a slave port of a next node or to one of said memory means (slave port of node containing bus 26).

Regarding Claim 2, Sindhu teaches the data processing system according to claim 1, characterized in that at each node means the number of said slave ports is higher than the number of said master ports (see Figure 1, where each node has at least two slave ports and at most one master port).

Regarding Claim 3, Sindhu teaches the data processing system according to claim 2, characterized in that said network of node means is hierarchically structured (see Figure 1, where three child nodes connect to one parent node, implying a hierarchy; also discussion of hierarchy on Column 5 Lines 14-19).

Regarding Claim 4, Sindhu teaches the data processing system according to claim 3, characterized in that said plurality of node means are arranged in a directed acyclic graph structure (see Figure 1 where the master ports of the node containing controllers 21 are connected to slave port of node containing bus 26; note that bus requests branch from nearest the processor at the cache level to farthest from the processor at main memory, rendering the graph directed, also see description of interconnection on Column 5 Lines 28-45).

Regarding Claim 5, Sindhu teaches the data processing system according to claim 4, characterized in that said plurality of node means are arranged in a tree structure (see Figure 1, where the child and parent nodes are arranged in a tree structure; also discussion of the tree structure in Column 5 first full paragraph).

Regarding Claim 6, Sindhu teaches the data processing system according to claim 1, characterized in that said plurality of node means include n groups of node means with n >= 2 (see Figure 1, where n = 2), wherein each of the slave ports of the node means of a first group (nodes containing busses 15) is connected to one of said plurality of data processing means (processing means containing caches 16), the master ports of the node means of the n^{th} group (nodes containing controllers 21) are coupled to said memory means (memory means containing controller 25 and main memory 13), and each of the slave ports of the node means of the nth group is connected to a master port of the node means of the $(n-1)^{th}$ group (the master port of the nodes containing busses 15 are connected to the slave port of the nodes containing controllers 21).

Regarding Claim 7, Sindhu teaches the data processing system according to claim 1, characterized in that said nodes means are hubs (nodes containing busses 15 as well as node containing bus 26).

Regarding Claim 8, Sindhu teaches the data processing system according to claim 1, characterized in that said communication interface means further includes at least one local memory unit adapted to be selectively accessed to by a memory request (RAMs 19).

Regarding Claim 9, Sindhu teaches the data processing system according to cleaim 8, characterized in that at least one node means further comprises at least one memory port to which a local memory unit is connected (see the port connecting RAMs 19 to controllers 21).

Regarding Claim 10, Sindhu teaches a data processing system according to claim 8, characterized in that said communication interface means includes a cache controller means for controlling at least a section of the local memory unit(s) as a cache memory (controller 21, also see Column 4 Lines 51-54).

Regarding Claim 11, Sindhu teaches the data processing system according to claim 1, characterized in that said communication interface means further includes at least one synchronization means for streaming communication between data processing means (arbiters 35 are such a synchronization means, see description of this device in the last paragraph of Column 7).

Regarding Claim 12, Sindhu teaches the data processing means according to claim 11, characterized in that at least one node means includes said synchronization means for streaming communication between the data processing means directly or indirectly coupled to said node means (arbiters 35 are indirectly coupled to the node means through caches 16, see Figure 1).

Regarding Claim 13, Sindhu teaches the data processing system according to claim 8, characterized in that the local memory units are configured to provide the storage means for a first-in/first-out function (which is well known in the art; see US 2002/0188811 Paragraph 0008) and said synchronization means comprises a first-in/first-out administration means for controlling said local memory unit(s) (the arbiter uses an algorithm that includes FIFO, see Column 8 Lines 18-24).

Regarding Claim 14, Sindu teaches the data processing system according to claim 1, characterized in that said communication interface means is provided on a single chip (providing circuitry on a chip is well known in the art).

Regarding Claim 15, Sindhu teaches the data processing system according to claim 14, characterized in that at least part of said plurality of data processing means is additionally provided on said single chip (providing circuitry on a chip is well known in the art).

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Harrington teaches a way of allowing access to a resource using a hierarchical structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Giardino whose telephone number is (571) 270-3565. The examiner can normally be reached on Monday-Thursday from 7:30 to 5:00. The examiner can also be reached on alternate Fridays from 7:30 to 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson, can be reached on Monday-Thursday from 7:30 to 5:00. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

8/22/2007

DAVID L. ROBERTSON
SUPERVISORY PATENT EXAMINER